IN THE SPECIFICATION

Please enter the following amendments to the Specification.

Please replace the original paragraph on page 7, line 26 through page 8, line 6 with the following replacement paragraph:

The cache 36 operates as a temporary buffer (i.e., volatile storage) for data elements 38, 42 exchanged between the external device 24 and the set of disk drives 32. When a copy of a data element 38 resides in the cache 36, the external device 24 can obtain the copy of the data element 38 from the cache 36 rather than retrieve the data element 38 from the set of disk drives 32. In some arrangements, the set of memory circuit boards 28 includes multiple memory circuit boards 28 for increased volatile storage capacity. When the set of memory circuit boards 28 includes multiple memory circuit boards 28, the cache 34 can be distributed across more than one memory circuit board 28 for load balancing purposes and/or fault tolerance.

Please replace the original paragraph on page 9, line 19 through page 10, line 3 with the following replacement paragraph:

Fig. 3 is a block diagram 60 of a memory circuit board 28 of the data storage system 22. The memory circuit board 28 includes an I/O port 62, a controller 64 and a set of memory locations 66. The I/O port 62 connects with a processor circuit board 50 (e.g., a front-end interface 26, a back-end interface 30, etc.) through the interconnection mechanism 34. The controller 64 includes a set of registers 68 (e.g., general purpose registers) which are capable of holding parameters used when the memory circuit board 28 performs particular instructions. The set of memory locations 66 includes an instruction library 70

and at least a portion 72 of the cache 36 (also see Fig. 1). The instruction library 70 includes sections of code which are staggered at set entry points. The controller 66 can jump to any of those entry points in order to execute particular sections of code at those entry points. The cache portion 72 forms at least a portion of the cache 36 and includes cache slots 74 for storing copies of data elements 38 stored in the set of disk drives 32 (also, see Fig. 1).

Please replace the original paragraph on page 15, line 17 through page 16, line 10 with the following replacement paragraph:

Fig. 6 shows a format 120 for the results in the above-described packaging arrangement. The format 120 includes a series of data element fields 122-A, 122-B, ... (e.g., blocks) for containing results of performing the individual instructions 94-1, 94-2, ... Each data element field 122 includes an SOF field 124 containing the unique start-of-file code, a payload field 126 containing a series of results, a set of additional fields 128 for control and status information, and an EOF field 130 for containing the unique end-of-file code. For example, the data element field 122-A includes an SOF field 124-A, a payload field 126-A, a set of additional fields 128-A and an EOF field 130-A. Similarly, the data element field 122-B includes an SOF field 124-B, a payload field 126-B, a set of additional fields 128-B and an EOF field 130-B, and so on. The payload field 126-A includes a series of results 126-1, 126-2, ... resulting from the controller 64 performing the series of operations based on the series of individual instructions 94 (Fig. 4). When the payload field 126-A is full or after a predetermined amount of time has elapsed from the time that the memory circuit board 28 received the communication 58 containing the SCRIPT command and series of individual instructions 94, the controller 64 of the memory circuit board 28 sends the data element 122-A back to the source of the communication 58 through the I/O port 62 (Fig. 3). Similarly, when the payload field 126-B of a next

data element 122-B is full or after another predetermined amount of time has elapsed, the controller 64 sends the data element 122-B to the source, and so on, until the memory circuit board 28 has completed the series of operations. In one arrangement, the controller 64 sends a final data element 122 to the source including any remaining unreported results in response to completing the series of operations rather than waiting for a predetermined amount of time to elapse.

IN THE TITLE

Please replace the original Title with the following new Title:

A DATA STORAGE SYSTEM HAVING AN IMPROVED MEMORY CIRCUIT BOARD CONFIGURED TO RUN SCRIPTS